In the Specification:

Amend the paragraph from page 7, line 29 to page 9, line 5 to read as follows:

Continuous time stage 16 includes a continuous time circuit that may be used for filtering the quantization error signal. According to one embodiment, the continuous time circuit comprises a first ~~order~~ filter and a second ~~order~~ filter that operate to low-pass filter a signal according to a desired response. For example, the first ~~order~~ filter may comprise a first capacitor that filters the quantized error signal according to a first low-pass response to yield a first filtered signal. The first capacitor may be selected such that the ratio between the capacitance of the first capacitor and the capacitance of the feedback capacitor are substantially greater than one. The second ~~order~~ may comprise a resistor and a second capacitor that filter the first filtered signal according to a second low-pass response to yield an integrated signal.

According to one embodiment, although the filtering performed by the first ~~order~~ filter and the second ~~order~~ filter may be characterized as low-pass filtering, the filters may generate an integrated signal if the filters operate at a high frequency. Continuous time stage 16 may include passive components such as resistors and capacitors in order to perform the filtering functions at high frequencies, thus enabling the sigma-delta modulator 10 to perform at high frequencies while consuming low power. Any other suitable passive components may be used to perform the continuous circuit functions without departing from the scope of the invention.

Quantizer ~~16~~ 18 digitizes the integrated signal to yield a digital signal corresponding to the sampled input analog signal. According to the illustrated embodiment, quantizer ~~16~~ comprises a comparator that amplifies the integrated signal

and compares the inputs to each other to generate a quantized signal. For example, the integrated signal may comprise two voltage signals that may be input at the comparator so that the voltage signals may be compared to each other and yield the digital output corresponding to the sampled analog signal. Quantizer 18 may comprise any other suitable one bit analog-to-digital converter without departing from the scope of the invention.

Amend the specification from page 11, line 17 to page 13, line 2 as follows:

According to the illustrated embodiment, the quantization error signals are filtered at ~~discrete~~ continuous time stage ~~16~~ by a first order low pass filter 14+24 and continuous time stage by another first order filter 26. First ~~order~~ filter 14+24 and the ~~a~~ second ~~order~~ filter 26 low-pass filter the quantization error signals If sigma-delta modulator 10 processes signals at high frequencies, first ~~order~~ filter 14+24 and second ~~order~~ filter 26 may operate as an integrator that integrates the quantization error signal without the use of operational amplifiers that may require a specific bandwidth and frequency of operation and power consumption as compared to a passive circuit as that illustrated.

First ~~order~~ filter 14+24 comprises a capacitor C_I and a switched feedback capacitor C_{RI} that filter the quantization error signal in a discrete time to yield a first filtered signal. The ~~First~~ capacitors C_I and C_{RI} may be directly coupled to summing node B to low-pass filter the quantization error signal. According to one embodiment, first capacitor C_I may be selected so that the ratio between first capacitor C_I and feedback capacitor C_{RI} satisfies Equation (1):

$$\frac{C_1}{C_{R1}} >>> 1 \quad (1)$$

so that the pole frequency ($f_{pole1} = \frac{f_{clk} C_{R1}}{C_1}$) of the first order filter can be set to be sufficiently low, where f_{clk} is the system clock rate and f_{pole1} is the pole frequency.

~~Second~~ The second first order filter 26 comprises a second capacitor C_2 and a second resistor R_2 that filter the first filtered signal in a continuous time to yield an integrated signal. According to the illustrated embodiment, second capacitor C_2 and a second resistor R_2 may be directly coupled to integration node C to filter the first filtered signal according to a low-pass response. Second capacitor C_2 and a second resistor R_2 may be selected according to a desired frequency response. According to the illustrated embodiment, second capacitor C_2 and a second resistor R_2 may be selected so that the frequency response substantially approximates a direct current (DC) frequency response with a pole close to zero frequency. For example, second capacitor C_2 and a second resistor R_2 may be selected according to Equation (2):

$$f_{pole2} = \frac{f_{clk} C_{R1}}{C_1} << f_{clk} \quad (2)$$

~~where DC is the DC frequency at which second order filter operates.~~ A stabilizing resistor R_0 may be used to increase the stability of the ~~continuous time circuit~~ overall modulator loop circuit. Any other suitable passive components may be used at continuous time circuit as well as at discrete time circuit and any additional or other filtering circuits may be used without departing from the scope of the invention.